

CLAIMS

What is claimed is:

1. A dynamically configurable logic gate comprising:
a controller configured to provide a first threshold reference signal;
an adder configured to sum the first threshold reference signal and at least one input signal to generate a summed signal;
a chaotic updater configured to apply a nonlinear function to the summed signal;
and
a subtractor configured to determine an output signal by taking a difference between a second threshold reference signal and the processed summed signal from said chaotic updater;
wherein the logic gate operates as one of a plurality of different logic gates responsive to adjusting at least one of the threshold reference signals.
2. The logic gate of claim 1, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as an AND logic gate.
3. The logic gate of claim 1, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as an OR logic gate.
4. The logic gate of claim 1, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as an XOR logic gate.
5. The logic gate of claim 1, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as a NOT logic gate.
6. The logic gate of claim 1, wherein the difference signal determined by said subtractor is an output signal of said logic gate.
7. A dynamically configurable logic gate comprising:
means for generating a first threshold reference signal;

means for adding the first threshold reference signal and at least one input signal to generate a summed signal;

means for applying a nonlinear function to the summed signal; and

means for determining a difference signal between a second threshold reference signal and the processed signal from said means for applying a nonlinear function to the summed signal;

wherein the logic gate operates as one of a plurality of different logic gates responsive to adjusting at least one of the threshold reference signals.

8. The logic gate of claim 7, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as an AND logic gate.

9. The logic gate of claim 7, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as an OR logic gate.

10. The logic gate of claim 7, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as an XOR logic gate.

11. The logic gate of claim 7, wherein at least one of the threshold reference signals is adjusted such that the logic gate operates as a NOT logic gate.

12. The logic gate of claim 7, wherein the difference signal determined by said means for determining a difference signal is an output signal of said logic gate.

13. A system for implementing a logical expression comprising:

a first dynamically configurable logic gate, wherein said first logic gate operates as one of a plurality of different logic gate types according to at least one provided reference signal; and

at least a second dynamically configurable logic gate, wherein said second logic gate operates as one of a plurality of different logic gate types according to at least one provided reference signal;

wherein the logical expression implemented by the system is altered responsive to modifying at least one of the reference signals provided to at least one of said dynamically configurable logic gates.

14. The system of claim 13, wherein said first and second dynamically configurable logic gates receive the same reference signal.

15. The system of claim 13, wherein said first and second dynamically configurable logic gates receive different reference signals.

16. The system of claim 13, wherein said first and second dynamically configurable logic gates are chaotic logic gates.

17. In a dynamically configurable logic gate, a method of changing the functionality of the logic gate comprising:

- generating a first threshold reference signal;

- adding the first threshold reference signal and at least one input signal to generate a summed signal;

- applying a nonlinear function to the summed signal;

- taking a difference between a second threshold reference signal and the processed summed signal; and

- changing the operation of the logic gate to function as one of a plurality of different logic gates responsive to adjusting at least one of the threshold reference signals.

18. The method of claim 17, wherein at least one of said threshold reference signals is adjusted such that the logic gate operates as an AND logic gate.

19. The method of claim 17, wherein at least one of said threshold reference signals is adjusted such that the logic gate operates as an OR logic gate.

20. The method of claim 17, wherein at least one of said threshold reference signals is adjusted such that the logic gate operates as an XOR logic gate.

21. The method of claim 17, wherein at least one of said threshold reference signals is adjusted such that the logic gate operates as a NOT logic gate.

22. The method of claim 17, wherein the difference signal is an output signal of said logic gate.